

EAST - [default.wsp:1]

File View Edit Tools Window Help

Pending

Active

- L1: (324919) memory
- L2: (16794) 1 and address\$3 with latch\$3
- L3: (7975) 2 and address\$3 with clock\$3
- L4: (3288) 3 and strobe
- L5: (1313) 3 and strobe with latch\$3
- L6: (0) 5 and bypass\$3 with parallel\$3 with (delay\$3 or register)
- L7: (0) 5 and by-pass\$3 with parallel\$3 with (delay\$3 or register)
- L8: (59) 5 and bypass\$3 with (delay\$3 or register)
- L9: (1) 5 and by-pass\$3 with (delay\$3 or register)
- L10: (0) 5 and by-pass\$3 with (delay\$3 or register) with read\$3
- L11: (20) 5 and bypass\$3 with (delay\$3 or register) with read\$3

Failed

Saved

Favorites

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Plurals Synonym

Default Highlight all hit terms initial

5 and bypass\$3
with (delay\$3
or register)
with read\$3

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6175891 B1	20010116	52	System and method for assigning addresses to	711/5	711/148 ; 711/202
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6141725 A	20001031	54	Updating a local memory based on information	711/100	345/430 ; 711/118
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6078985 A	20000620	55	Memory system having flexible addressing and	711/5	711/218
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6073204 A	20000606	59	Memory system having flexible architecture and	711/100	365/185.08 ; 365/189.01
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6021459 A	20000201	56	Memory system having flexible bus structure and	711/5	365/230.03 ; 365/230.06
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6000019 A	19991207	52	SDRAM data allocation system and method utilizing dual	711/157	711/104 ; 711/118
7	<input type="checkbox"/>	<input type="checkbox"/>	US 5974499 A	19991026	66	Memory system having read modify write function and	711/103	
8	<input type="checkbox"/>	<input type="checkbox"/>	US 5917772 A	19990629	13	Data input circuit for	365/230.06	365/189.01

Start Inbox - Microsoft Outlook EAST - [default.wsp:1] 4:59 PM

EAST - [default.wsp.1]

File View Edit Tools Window Help

Pending

Active

- L1: (322125) memory
- L2: (919) 1 and address\$3 with latch\$3 with delay\$3
- L3: (625) 2 and address\$3 with clock
- L4: (179) 3 and data with strobe
- L5: (0) 4 and bypass\$3 with delay\$3 with read\$3
- L6: (3) 2 and bypass\$3 with delay\$3 with read\$3
- L7: (247) 1 and address\$3 with latch\$3 with delay\$3 with clock
- L8: (1) 7 and bypass\$3 with delay\$3 with read\$3
- L9: (1) 2 and bypass\$3 adj3 delay\$3 with read\$3
- L10: (33) 1 and bypass\$3 adj3 delay\$3 with read\$3
- L11: (7) 1 and bypass\$3 adj3 delay\$3 with read\$3 with address\$3
- L12: (0) 1 and bypass\$3 adj3 delay\$3 adj circuit with read\$3 with address\$3
- L14: (379299) memory
- L16: (0) 15 and bypass\$3 adj3 delay\$3 with read\$3 with address\$3
- L15: (25) 14 and address\$3 with latch\$3 with delay\$3 with clock

Failed

Saved

14 and address\$3 with latch\$3 with delay\$3 with clock

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 4415984 A	19831115	9	Synchronous clock regenerator for binary		
2	<input type="checkbox"/>	<input type="checkbox"/>	EP 260039 A1	19880316	18	Dynamic random access memory.		365/182
3	<input type="checkbox"/>	<input type="checkbox"/>	US 5633833 A	19970527	9	Address buffer for blocking noise		
4	<input type="checkbox"/>	<input type="checkbox"/>	JP 57138291 A	19820826	5	CONTROL SYSTEM FOR TIME-DIVISION MULTIPLEX		
5	<input type="checkbox"/>	<input type="checkbox"/>	JP 58149540 A	19830905	8	CONTROL STORAGE DEVICE		
6	<input type="checkbox"/>	<input type="checkbox"/>	JP 60083101 A	19850511	5	PROCESS CONTROLLER		700/76

Hits Details

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File View Edit Tools Window Help

Drafts
Pending
Active
L1: (334605) memory
L2: (17091) 1 and address\$3 with latch\$3
L3: (8124) 2 and address\$3 with clock\$3
L4: (2021) 3 and strobe with data
L5: (183) 3 and strobe with data with clock\$3 with latch\$3
L6: (0) 5 and address\$3 with delay\$3 with (bypass\$3 or by-pass\$3)
L7: (91) 5 and shift adj register
L8: (24) 7 and (bypass\$3 or by-pass\$3)
Failed
Saved
Favorites
Tagged
UDC
Queue
Trash

Search List Browse
DB4 Plads Synops
Default Highlight all hit terms in bold
7 and (bypass\$3 or by-pass\$3)

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 5995424 A	19991130	75	Synchronous memory test system	365/201	365/189.05 ; 365/194
2	<input type="checkbox"/>	<input type="checkbox"/>	US 5914902 A	19990622	76	Synchronous memory tester	365/201	365/222 ; 365/233
3	<input type="checkbox"/>	<input type="checkbox"/>	US 5757794 A	19980526	43	Digital down converter and method	370/362	710/107
4	<input type="checkbox"/>	<input type="checkbox"/>	US 5633815 A	19970527	43	Formatter	708/204	708/550
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5617344 A	19970401	43	Fixed coefficient high decimation filter	708/313	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 5570392 A	19961029	43	Phase generator	375/308	332/104